

REMARKS

Claims 1-20 remain in the application for consideration of the Examiner.

Reconsideration and withdrawal of the outstanding rejections and objections are respectfully requested in light of the above amendments and following remarks.

Turning now to the art rejections, Claims 1-9, 11, and 14-19 were rejected under 35 U.S.C. § 102(e) as being anticipated by Fujioka; and Claims 10, 12, 13, and 20 were rejected under 35 U.S.C. § 103 as being unpatentable over Fujioka in view of Cartwright.

These rejections are respectfully traversed.

It is respectfully submitted that Fujioka does not disclose or suggest the presently claimed invention including the temperature responsive unit having a second voltage temperature response modeled on the first voltage temperature response as defined in the various forms in independent Claims 1 and 14.

Fujioka discloses that the drain and gate electrodes of the nMOS transistor 64 are short-circuited in order to prevent the internal power-supply V_{ii} from changing according to ambient temperature and does not disclose modeling.

However, this does not disclose the above mentioned subject matter.

Cartwright does not cure the above noted defects.

In light of the above, it is respectfully submitted that the present application is in condition for allowance, and notice to that effect is respectfully requested.

While it is believed that the instant response places the application in condition for allowance, should the Examiner have any further comments or suggestions, it is respectfully requested that the Examiner contact the undersigned in order to expeditiously resolve any outstanding issues.

To the extent necessary, Applicant petitions for an Extension of Time under 37 CFR 1.136. Please charge any fees in connection with the filing of this paper, including extension of time fees, to the deposit account of Texas Instruments Incorporated, Account No. 20-0668.

Respectfully submitted,



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